CLAIMS

1. A method of forming a semiconductor structure comprising:

providing a substrate;

forming a control electrode overlying said substrate, said control electrode including a sidewall;

forming an insulating layer that is adjacent to said control electrode and overlying said substrate;

forming a sidewall spacer around said sidewall of said control electrode and in contact with said insulating layer;

forming a current electrode diffusion region in said substrate substantially aligned to said sidewall spacer;

exposing the semiconductor structure to a gaseous fluorine ambient to substantially remove said sidewall spacer; and

forming an extension region to said current electrode diffusion region in said substrate, said extension region substantially aligned to said control electrode.

2. The method of claim 1, further comprising implementing said insulating layer as an oxide layer.

3. The method of claim 1, further comprising implementing the sidewall spacer from at least one of silicon, silicon germanium, or germanium.

4. The method of claim 1, further comprising implementing said gaseous fluorine ambient with molecular fluorine.

5. The method of claim 1, further comprising implementing said gaseous fluorine ambient with atomic fluorine.

6. The method of claim 5, further comprising generating said atomic fluorine from a plasma.

7. The method of claim 6, further comprising implementing said plasma from at least one of nitrogen trifluoride, xenon difluoride or molecular fluorine.

8. The method of claim 1, further comprising:

exposing the semiconductor structure to said gaseous fluorine ambient to substantially remove said sidewall spacer without substantially modifying said insulating layer.

9. The method of claim 1, further comprising:

etching said sidewall spacer with said gaseous fluorine ambient selective to said insulating layer.

10. The method of claim 9, further comprising:

etching said sidewall spacer with said gaseous fluorine ambient selective to said insulating layer by a factor of at least fifty to one.

11 The method of claim 1, further comprising:

surrounding the semiconductor structure with a dielectric isolation region.

12. The method of claim 11, further comprising:

exposing the semiconductor structure to said gaseous fluorine ambient to substantially remove said sidewall spacer and to introduce fluorine into said dielectric isolation region.

13. The method of claim 11, further comprising:

exposing said dielectric isolation region to a gas to improve insulating characteristics of said dielectric isolation region.

14. A method of forming a semiconductor structure comprising:

providing a substrate;

introducing a dielectric region within the substrate to laterally electrically isolate the semiconductor structure;

forming a control electrode overlying said substrate, said control electrode including a sidewall;

forming an insulating layer that is adjacent to said control electrode and overlying said substrate;

forming a sidewall spacer around said sidewall of said control electrode and in contact with said insulating layer;

forming a current electrode diffusion region in said substrate substantially aligned to said sidewall spacer;

exposing the semiconductor structure to a gaseous fluorine ambient to substantially remove said sidewall spacer and to add fluorine to said dielectric region; and

forming an extension region to said current electrode diffusion region in said substrate, said extension region substantially aligned to said control electrode.

15. The method of claim 14, further comprising implementing the dielectric region as an oxide layer.

16. The method of claim 14, further comprising implementing the gaseous fluorine ambient as molecular fluorine.

17. The method of claim 14, further comprising implementing the gaseous fluorine ambient as atomic fluorine.

18. The method of claim 17, further comprising generating said atomic fluorine from plasma.

19. The method of claim 18, further comprising implementing said plasma as at least one of nitrogen trifluoride, xenon difluoride or molecular fluorine.

20. The method of claim 19, further comprising implementing said dielectric region as an oxide layer.

21. A method of forming a semiconductor structure comprising:

providing at least two semiconductor structures;

laterally isolating said at least two semiconductor structures with a dielectric region; and

exposing said at least two semiconductor structures including said dielectric region to a gaseous fluorine ambient, the dielectric region having a resulting lower dielectric constant.

22. The method of claim 21, wherein a first semiconductor structure and a second semiconductor structure of said at least two semiconductor structures are laterally adjacent.

23. A semiconductor structure comprising:

a substrate having an overlying dielectric layer;

a control electrode overlying said substrate and separated from the substrate by the dielectric layer, said control electrode including a sidewall;

an insulating layer adjacent to said sidewall of said control electrode and at least a portion of said substrate;

a sidewall spacer adjacent to said insulating layer which is adjacent to said sidewall of said control electrode and said substrate;

a current electrode diffusion region portion substantially aligned to said control electrode; and

an isolating region surrounding the semiconductor structure, said isolating region comprised of a dielectric comprised of fluorine.

24. A structure comprising:

a substrate;

at least a first semiconductor structure and a second semiconductor structure which are laterally adjacent and a portion of each of the first semiconductor structure and the second semiconductor structure formed within the substrate; and

a dielectric region laterally isolating said first semiconductor structure from said second semiconductor structure,

wherein said dielectric region comprises fluorine.

25. The structure of claim 24, wherein at least the first semiconductor structure further comprises:

a control electrode overlying said substrate and insulated therefrom by a dielectric, said control electrode including a sidewall;

an insulating layer adjacent said sidewall of the control electrode and at least a portion of said substrate;

a sidewall spacer adjacent to said insulating layer which is adjacent to said sidewall of the control electrode; and

a current electrode diffusion region in said substrate substantially aligned to said sidewall spacer.